What is Claimed is:

1. A circuit for correcting a duty factor of a clock signal, comprising:

a phase comparator for detecting a phase difference of an input clock signal having a duty factor to be corrected, and a corrected clock signal having the duty factor corrected, and generating a shift control signal;

a control signal generating part for shifting a clock generating reference signal in response to the shift control signal, and delaying the clock generating reference signal for a preset time period to generate 180° and 360° clock generating control signals; and

a clock signal generating part for generating a clock signal having a corrected duty factor according to the 180° and 360° clock generating control signals.

2. The circuit as claimed in claim 1, wherein the corrected clock signal provided to the phase comparator is corrected such that a duty factor thereof is 50%.

3. The circuit as claimed in claim 1, wherein the control signal generating part shifts the clock generating reference signal in left/right direction.

4. The circuit as claimed in claim 1, wherein the control signal generating part delays a preset time period set according to a shifted position of the clock generating reference signal.

5. The circuit as claimed in claim 1, wherein the control signal generating part includes;

a shift register for shifting the clock generating reference signal in a left/right direction in response to a shift control signal,

a synchronized signal providing part for synchronizing a shifted clock generating reference signal to the input clock signal,

a first delay loop for delaying the synchronized clock generating reference signal for a preset time period, to provide as a 180° clock generating phase signal, and

a second delay loop for delaying the synchronized clock generating reference signal for a preset time period, to provide as a 360° clock generating phase signal.

6. The circuit as claimed in claim 5, wherein the shift register stores a high voltage as the clock generating reference signal, and shifts the clock generating reference signal.

7. The circuit as claimed in claim 5, wherein the first delay loop delays the clock generating reference signal for a preset time period set according to a shifted position of the clock generating reference signal.

8. The circuit as claimed in claim 5, wherein the second delay loop delays the clock generating reference signal for a time period two times longer than a delay time period delayed by the first delay loop.

9. The circuit as claimed in claim 5, wherein the first or second loop includes a plurality of delays disposed between output terminals of the synchronized signal providing part.

10. The circuit as claimed in claim 1, wherein the clock signal generating part includes;

a correction delay for delaying the 360° clock generating control signal,

a first pulse signal generator for generating a pulse signal in response to the 360° clock generating control signal delayed at the correction delay,

a second pulse signal generator for generating a pulse signal in response to the 180° clock generating control signal, and

a corrected clock signal generator for generating clock signals respectively having 360° and 180° phases in response to the pulse signals from the first pulse signal generator and the second pulse signal generator.

11. The circuit as claimed in claim 10, wherein the correction delay delays a time period required from a time the first and second pulse signal generators generate pulse signals to a time the clock signal generating part generates clock signals having 360° and 180° in response to the generated pulse signals.

12. The circuit as claimed in claim 10, wherein the first or second pulse signal generator includes a first inverter group for delaying and inverting an output signal from the correction delay or the 180° clock generating control signal from the control signal generating part,

an NAND gate having a first terminal for receiving the output signal from the correction delay or the 180° clock generating control signal from the control signal generating part and a second terminal for receiving an output signal from the first inverter group, and

a second inverter group for delaying and inverting an output signal from the NAND gate.

13. The circuit as claimed in claim 12, wherein the first inverter group includes three inverters connected in series.

14. The circuit as claimed in claim 12, wherein the second inverter group includes one inverter.

15. The circuit as claimed in claim 10, wherein the corrected clock signal generator includes;

first and second transistors connected between power terminal Vdd and a ground in series, for receiving an output signal from the first and second pulse signal generators, and

a plurality of inverters connected between the first and the second transistors.

16. The circuit as claimed in claim 15, wherein the first transistor is a PMOS transistor, and the second transistor is an NMOS transistor.

17. The circuit as claimed in claim 15, wherein the first transistor has a gate connected to an inverter for receiving an inverted output signal of the first pulse signal generator, and the second transistor has a gate connected to received the output signal of the second pulse signal generator.

18. The circuit as claimed in claim 15, wherein the plurality of inverters are first, second and third inverters, wherein the first and second inverters are connected in parallel to serve as a latch, and the third inverter is connected in series to the first or second inverter.